

**PES UNIVERSITY**

***(Established under Karnataka Act No. 16 of 2013)***

***100 ft Ring Road Campus, Bengaluru – 560 085, Karnataka, India***

*Project report on*

“Designing a 3x3 - Matrix Inversion in System Verilog and Implementing 2x2 -Matrix Inversion on the Xilinx Artix 7 series FPGA”

**Submitted by**

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***For the partial fulfilment of the course CADD***

***(Computer Aided Digital Design)***

**UE22EC252A**

Electronics and Communication Engineering

**Submitted to**

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Faculty of Engineering

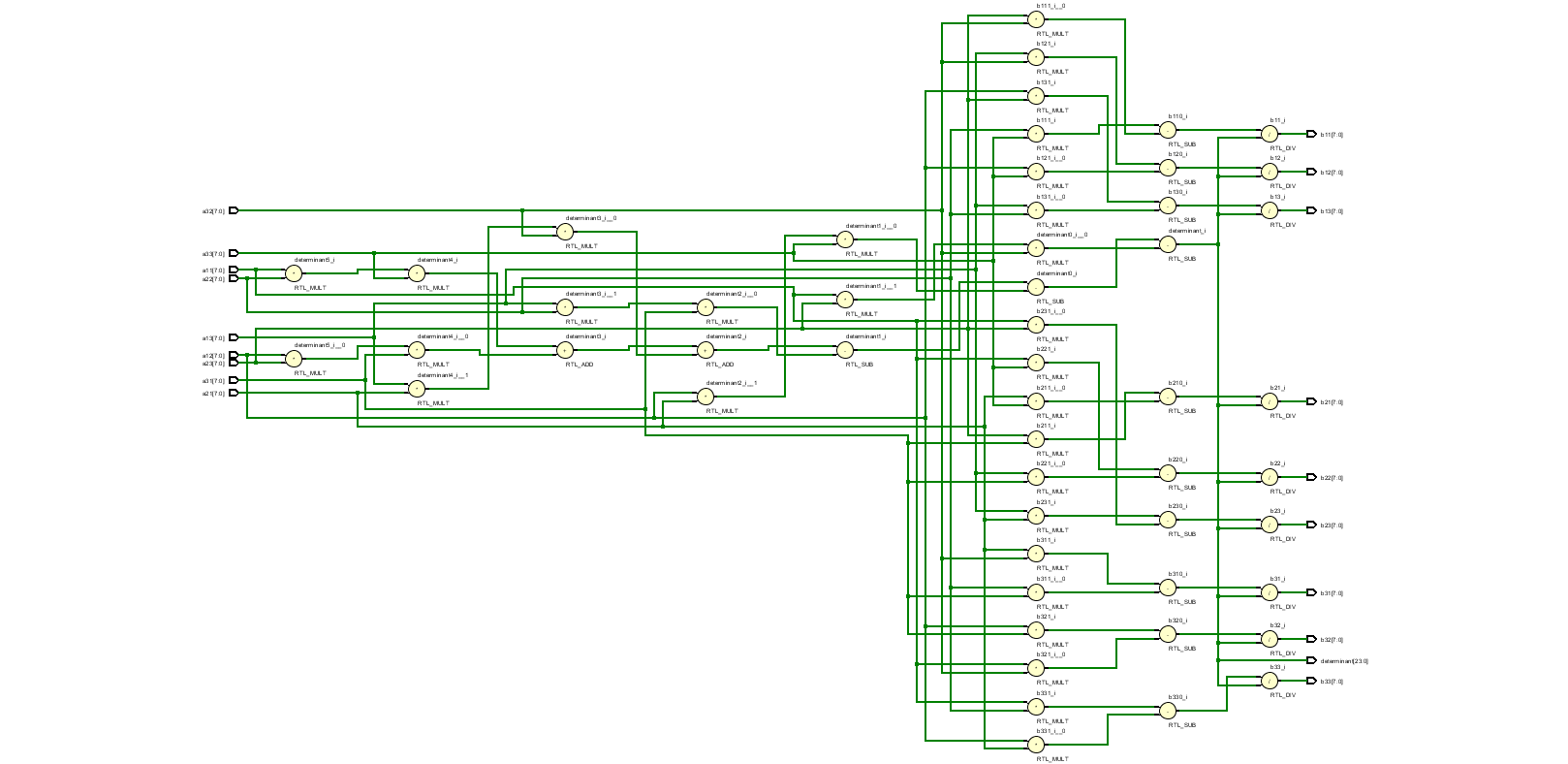
(Program: B.tech)

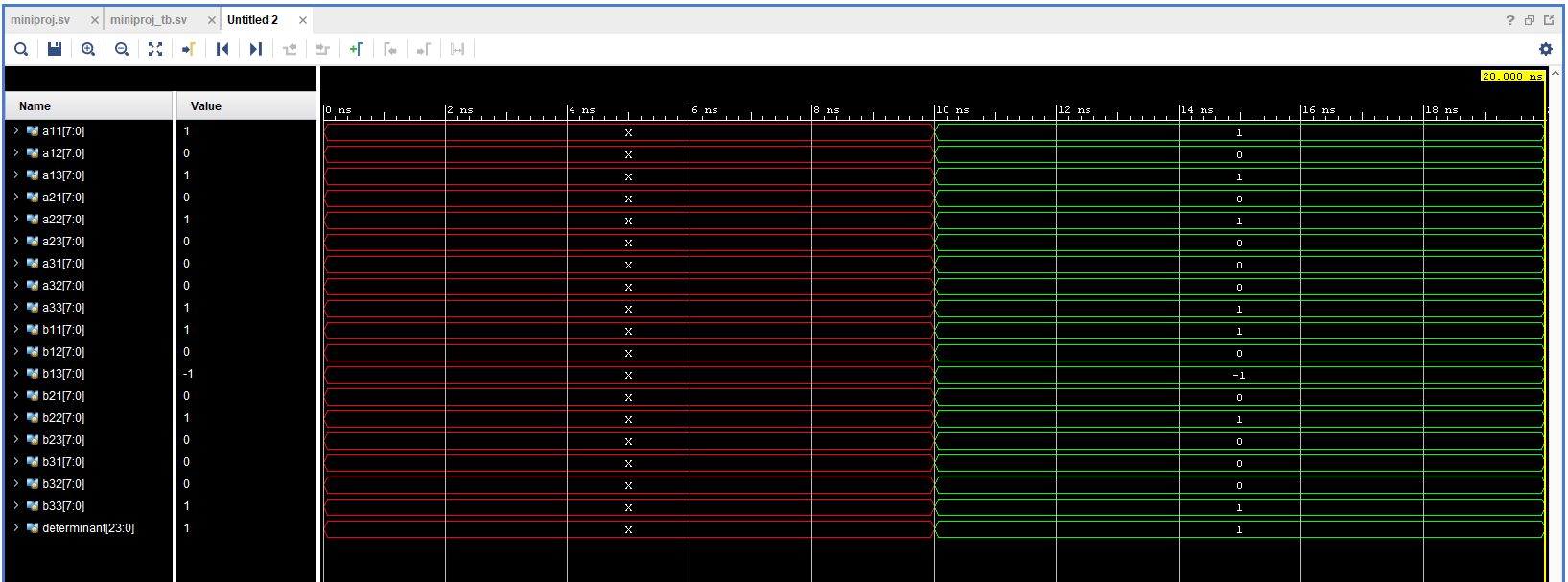
MATRIX INVERSION

TRUTH TABLE:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Column | a1 | a2 | a3 | b1 | b2 | b3 | determinant |
| 1 | 1 | 0 | 1 | 1 | 0 | -1 |  |
| 2 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 3 | 0 | 0 | 1 | 0 | 0 | 1 |  |

(These designs are of 3x3 matrix inversion on this page)

RTL SCHEMATIC:

SIMULATION GRAPH:

AIM: Simulation and Implementation of Matix Inversion (3x3)

DESIGN CODE:

module matrix\_inversion(

input logic signed [7:0] a11, a12, a13,

input logic signed [7:0] a21, a22, a23,

input logic signed [7:0] a31, a32, a33,

output logic signed [7:0] b11, b12, b13,

output logic signed [7:0] b21, b22, b23,

output logic signed [7:0] b31, b32, b33,

output logic [23:0] determinant);

assign determinant = (a11 \* a22 \* a33) + (a12 \* a23 \* a31) + (a13 \* a21 \* a32) - (a13 \* a22 \* a31) - (a12 \* a21 \* a33) - (a11 \* a23 \* a32);

assign b11 = ((a22 \* a33 - a23 \* a32) / determinant);

assign b12 = ((a13 \* a32 - a12 \* a33) / determinant);

assign b13 = ((a12 \* a23 - a13 \* a22) / determinant);

assign b21 = ((a23 \* a31 - a21 \* a33) / determinant);

assign b22 = ((a11 \* a33 - a13 \* a31) / determinant);

assign b23 = ((a13 \* a21 - a11 \* a23) / determinant);

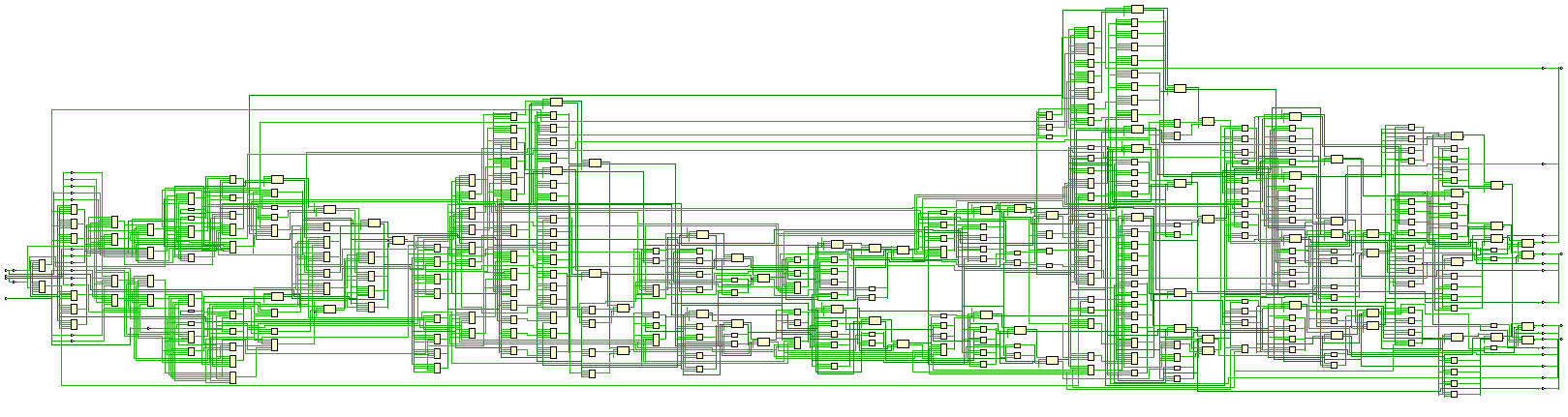
assign b31 = ((a21 \* a32 - a22 \* a31) / determinant);

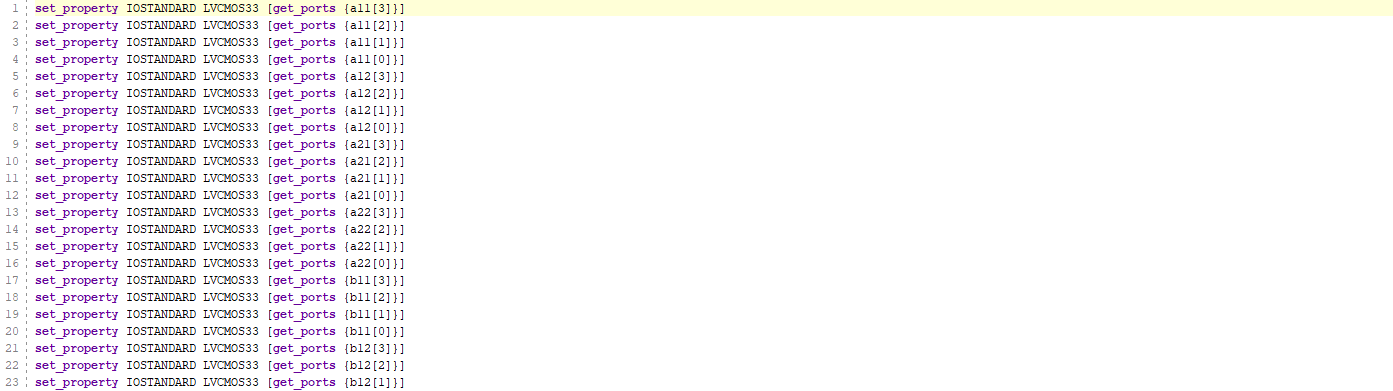
assign b32 = ((a12 \* a31 - a11 \* a32) / determinant);

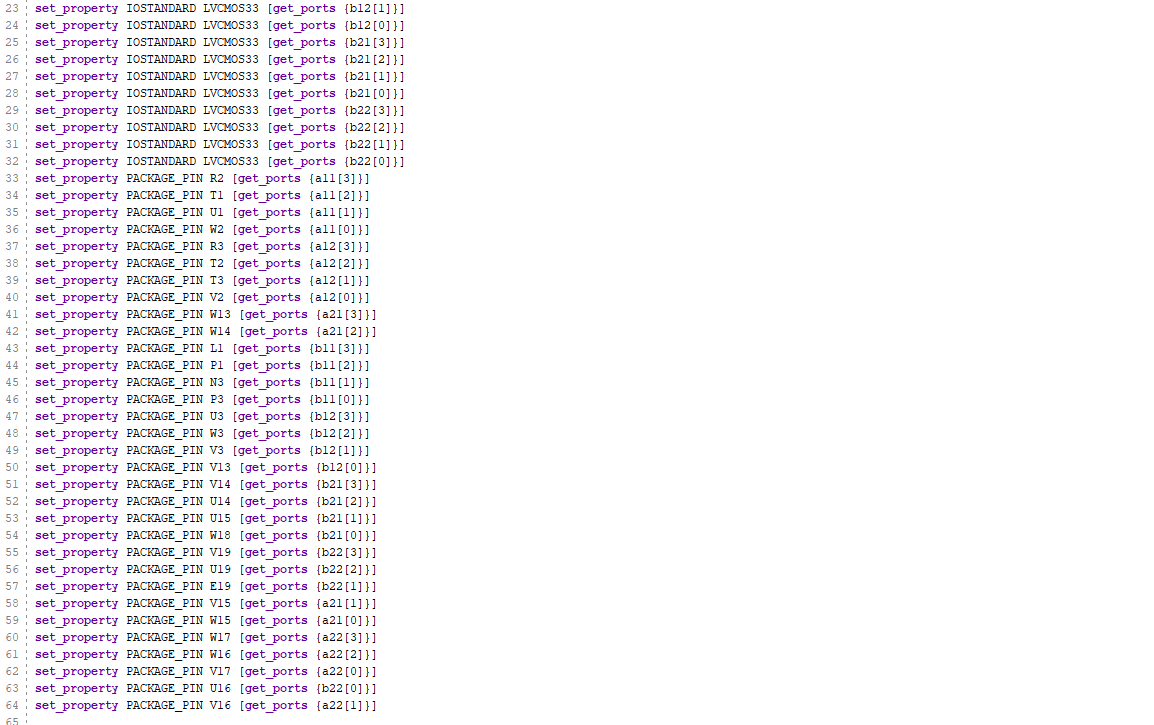
assign b33 = ((a11 \* a22 - a12 \* a21) / determinant);

end

endmodule

IMPLEMENTATION SCHEMATIC:

CONSTRAINTS:



(These designs are of 2x2 matrix inversion on this page)

TESTBENCH CODE:

module matrix\_inversion\_tb;

logic [7:0]a11,a12,a13,a21,a22,a23,a31,a32,a33,b11,b12,b13,b21,b22,b23,b31,b32,b33;logic [23:0] determinant;

// Instantiate the module to be tested

matrix\_inversion dut ( a11, a12, a13, a21, a22, a23, a31, a32, a33, b11, b12, b13, b21, b22, b23, b31, b32, b33,determinant);

initial begin

#10 a11 = 1; a12 = 0; a13 = 1;

a21 = 0; a22 = 1; a23 = 0;

a31 = 1; a32 = 0; a33 = 1;

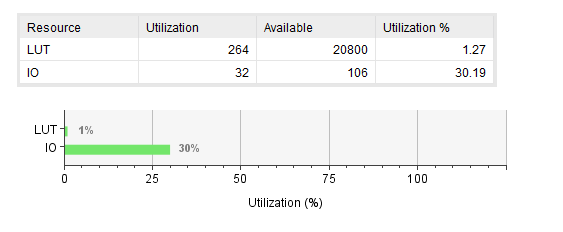
#10;

$finish;

end

endmodule

UTILIZATION REPORT:



(These designs are of 2x2 matrix inversion on this page)

LIMITATIONS:

* Floating numerical cannot be displayed on simulation and FPGA Board.
* 3x3 matrix need minimum of 18 inputs but FPGA Board has only 16 inputs.
* In FPGA Board 2x2 matrix (4-bit signed) can be displayed with the first limitation.

RESULT: Matrix Inversion 3x3 simulation and 2x2 implementation verified.